

What is claimed is:

1 1. A method for charge control of a photoflash
2 capacitor comprising the steps of:

3 generating an input current to induce a charge current
4 for the photoflash capacitor when an activation
5 signal is asserted;

6 detecting a first voltage from the photoflash capacitor
7 and a second voltage corresponding to the input
8 current;

9 asserting and de-asserting a recharge signal when the
10 first detected voltage is lower and higher than a
11 first reference voltage, respectively;

12 asserting and de-asserting a current limit signal when
13 the second detected voltage is higher and lower
14 than a second reference voltage, respectively;

15 asserting the activation signal only when the recharge
16 signal is asserted and the current limit signal
17 is de-asserted; and

18 providing a pin for connection of a resistive element
19 which determines the second reference voltage.

1 2. The method as claimed in claim 1, wherein the
2 input current is generated by the activation signal closing
3 a switch to form a loop on a primary side of a transformer
4 and cut off by the activation signal opening the switch.

1 3. The method as claimed in claim 1 further
2 comprising the step of generating a constant current flowing
3 through the resistive element, wherein the second reference

4 voltage is a voltage difference across the resistive
5 element.

1 4. A photoflash capacitor charger operating in
2 conjunction with a microprocessor, comprising:
3 a transformer generating an input current to induce a
4 charge current for a photoflash capacitor when an
5 activation signal is asserted;
6 a recharge controller detecting a first voltage from
7 the photoflash capacitor, and asserting and de-
8 asserting a recharge signal when the first
9 detected voltage is lower and higher than a first
10 reference voltage, respectively; and
11 a current limiter detecting a second voltage
12 corresponding to the input current, asserting and
13 de-asserting a current limit signal respectively
14 when the second detected voltage is higher and
15 lower than a second reference voltage, and
16 asserting the activation signal only when the
17 recharge signal is asserted and the current limit
18 signal is de-asserted;
19 wherein the second reference voltage is determined by
20 the microprocessor.

1 5. The photoflash capacitor charger as claimed in
2 claim 4, wherein the current limiter comprises:
3 a comparator circuit asserting and de-asserting the
4 current limit signal respectively when the
5 detected voltage is higher and lower than the
6 reference voltage; and

7 an SR latch asserting the activation signal if the
8 recharge signal is asserted and the current limit
9 signal is de-asserted, otherwise, de-asserting
10 the activation signal.

1 6. The photoflash capacitor charger as claimed in
2 claim 5, wherein the comparator circuit comprises:
3 a current source;
4 a resistive element having a first end coupled to the
5 current source and a second end coupled to a
6 ground; and
7 a comparator having a positive input coupled to the
8 first end of the resistive element and a negative
9 input receiving the second detected voltage, and
10 outputting the current limit signal;
11 wherein the resistive element is adjustable.

1 7. The photoflash capacitor charger as claimed in
2 claim 4 further comprising a switch coupled in a path of the
3 input current, closed and opened respectively when the
4 activation signal is asserted and de-asserted.

1 8. The photoflash capacitor charger as claimed in
2 claim 4 further comprising a resistor coupled in a path of
3 the input current, wherein the second detected voltage is a
4 voltage difference across the resistor.

1 9. An integrated circuit for charge current limit of
2 a photoflash capacitor, comprising:
3 first, second, third and fourth pins respectively for
4 reception of a ground voltage, first detected

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5 voltage from the photoflash capacitor and
6 connection with a resistive element and a
7 transformer;
8 a switch connected with a resistor in series between
9 the fourth and first pin;
10 a recharge controller connected to the second pin for
11 assertion and de-assertion of a recharge signal
12 respectively when the first detected voltage is
13 lower and higher than a first reference voltage;
14 a comparator circuit comprising:
15 a current source connected to the third pin; and
16 a comparator having a positive input connected to
17 the third pin and a negative input connected
18 where the switch and resistor is connected;
19 and
20 an SR latch having a set input connected to the
21 recharge controller for reception of the recharge
22 signal, a reset input connected to an output of
23 the comparator and an output connected to a
24 control node of the switch.

1 10. The integrated circuit as claimed in claim 9,
2 wherein the switch is a transistor.